What is claimed is:

1. A method of maintaining photolithographic precision alignment for a wafer after it is bonded comprising the steps:
   a. at first making an alignment marks on the surface of a bottom wafer and then a microstructure for the device;
   b. forming two cavities on the rear surface of a top wafer at the position corresponding to said alignment marks by an etching process;
   c. applying grinding process to said wafer after completion of bonding said top and said bottom wafers;
   d. exposing said alignment marks made on said bottom wafer by grinding said top wafer to reduce its thickness;

   by doing so, facilitating an exposure equipment to find out said alignment marks so as to carry out successive electrical circuit layout process conveniently.
2. The method as in claim 1, wherein said exposure equipment maintains precision of photolithographic alignment with respect to said alignment marks made on said bottom wafer.
3. The method as in claim 1, wherein said top and said bottom wafers are a n-type wafer and p-type wafer respectively.
4. The method of claim 1, wherein said cavities formed on said top wafer are performed by either wet or dry etching.
5. The method of claim 1, wherein said cavity formed on said top wafer can be of any shape as long as it is able to expose said alignment marks made

on said bottom wafer after said top wafer thickness is reduced by thinning process.